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10/649,565	08/26/2003	Naveen Kumar Vandanapu	42P16529	5944

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EXAMINER	
DO, CHAT C	
ART UNIT	**PAPER NUMBER**
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/649,565	VANDANAPU, NAVEEN KUMAR	
	Examiner	Art Unit	
	Chat C. Do	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 August 2003 and 10 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-44* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *08/26/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 39 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The term "can" in line 4 is a relative term which renders the claim indefinite. The term "can" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

Claim Rejections - 35 USC § 101

3. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

4. Claims 1-41 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claims 1-41 cite a method, article, and system for searching a set of ratio in accordance with a mathematical algorithm. However, claims 1-41 merely disclose steps/components for searching a set of ratio without further disclosing a

practical/physical application and further the claims appear to preempt every substantial practical application of the idea embodied by the claim and there is no cited limitation in the claims that breathes sufficient life and meaning into the preamble so as to limit it to a particular practical application rather than being so broad and sweeping as to cover every substantial practical application of the idea embodied therein. In addition, claims 16-23 are directed to a non-tangible medium as propagated signal...as cited in original specification page 7 lines 13-21. Therefore, claims 1-41 are directed to non-statutory subject matter.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-4, 6-17, and 19-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art in view of de Tremiolles et al. (U.S. 6,748,405).

Re claim 1, the admitted prior art discloses in pages 2-4 a method for searching (e.g. paragraph [0002]), comprising: a set of ratios (e.g. expressions 1-4); computing in processing blocks a set of values derived from a set of ratios, each value of the set computed by a respective processing block (e.g. computing the product terms in either expression 3/4); comparing in the processing blocks the respective computed value against a predetermined value accessible by the respective processing block (e.g.

compare against zero as threshold as seen in expression 3/4); selecting one of the computed value and the predetermined value for a respective processing block that is nearer to an optimum value (e.g. page 4 lines 1-4); and determining which of the selected values among the processing blocks is nearest to the optimum value (e.g. page 4 lines 2-6).

The admitted prior art fails to disclose the step of splitting among parallel processing blocks elements of a set of values derived form a set of number and perform other steps in parallel to determine the final optimum value. However, De Tremiolles et al. disclose in Figures 2 and 4 the step of splitting among parallel processing blocks elements of a set of values derived form a set of number (e.g. by step A in Figure 4) and perform other steps in parallel (e.g. Figure 2 and step B to F) to determine the final optimum value (e.g. output of step G in Figure 4).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add the step of splitting among parallel processing blocks elements of a set of values derived form a set of number and perform other steps in parallel to determine the final optimum value as seen in De Tremiolles et al.'s invention into the admitted prior art's invention because it would enable to increase/improve the response time by processing in parallel (e.g. col. 1 lines 10-16 and col. 2 lines 63-65).

Re claim 2, the admitted prior art fails to disclose in pages 2-4 splitting among parallel processing blocks elements of a set of values derived form a set of ratios comprises splitting among the parallel processing blocks a set of pre-computed values

derived from the set of ratios, each pre-computed value of the set associated with a respective processing block. However, De Tremiolles et al. disclose in Figures 2 and 4 splitting among parallel processing blocks elements of a set of values derived form a set of ratios comprises splitting among the parallel processing blocks a set of pre-computed values derived from the set of ratios, each pre-computed value of the set associated with a respective processing block (e.g. wherein pre-computed value is one of the set of P Numbers as clearly addressed in abstract).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add splitting among parallel processing blocks elements of a set of values derived form a set of ratios comprises splitting among the parallel processing blocks a set of pre-computed values derived from the set of ratios, each pre-computed value of the set associated with a respective processing block as seen in De Tremiolles et al.'s invention into the admitted prior art's invention because it would enable to increase/improve the response time by processing in parallel (e.g. col. 1 lines 10-16 and col. 2 lines 63-65).

Re claim 3, the admitted prior art further discloses in pages 2-4 the set of values derived from a set of ratio and each value of the set computed by a respective processing block (e.g. expression 3-4 in page 3).

The admitted prior art fails to disclose splitting among parallel processing blocks elements of a set of values comprises computing in parallel processing blocks the set of values. However, De Tremiolles et al. disclose in Figures 2 and 4 splitting among parallel processing blocks elements of a set of values (e.g. by step A in Figure 4)

comprises computing in parallel processing blocks the set of values (e.g. Figures 2 and steps B to F).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add the step of splitting among parallel processing blocks elements of a set of values comprises computing in parallel processing blocks the set of values as seen in De Tremiolles et al.'s invention into the admitted prior art's invention because it would enable to increase/improve the response time by processing in parallel (e.g. col. 1 lines 10-16 and col. 2 lines 63-65).

Re claim 4, the admitted prior art further discloses in pages 2-4 computing the set of values derived from the set of ratios comprises creating a ratio of an element at an index of a first buffer to an element at a corresponding index of a second buffer (e.g. page 3).

Re claim 6, the admitted prior art further discloses in pages 2-4 comparing the computed value to the predetermined value comprises comparing the computed ratio to a predetermined ratio (e.g. expressions 3-4 in page 3).

Re claim 7, the admitted prior art further discloses in pages 2-4 comparing the computed ratio to the predetermined ratio further comprises: generating a first product of the numerator of the computed ratio multiplied by the denominator of the predetermined ratio; generating a second product of the numerator of the predetermined ratio multiplied by the denominator of the computed ratio; and determining whether the first product minus the second product is greater than zero (e.g. expression 3 in page 3).

Re claim 8, the admitted prior art further discloses in pages 2-4 selecting one of the computed value and the predetermined value that is nearer to the optimum value comprises selecting the computed value if the first product minus the second product is greater than zero, otherwise selecting the predetermined value (e.g. paragraph [0005]).

Re claim 9, the admitted prior art further discloses in pages 2-4 comparing the computed ratio to the predetermined ratio further comprises: generating a first product of the numerator of the computed ratio multiplied by the denominator of the predetermined ratio; generating a second product of the numerator of the predetermined ratio multiplied by the denominator of the computed ratio; and determining whether the first product minus the second product is less than zero (e.g. expression 4 in page 3).

Re claim 10, the admitted prior art further discloses in pages 2-4 selecting one of the computed value and the predetermined value that is nearer to the optimum value comprises selecting the computed value if the first product minus the second product is less than zero, otherwise selecting the predetermined value (e.g. paragraph [0005]).

Re claim 11, the admitted prior art further discloses in pages 2-4 comparing the ratio to the predetermined value comprises comparing the ratio to an initial-value ratio for the respective processing block (e.g. wherein the initial-value is the predetermined min or max values in expression 3 or 4 in page 3).

Re claim 12, the admitted prior art further discloses in pages 2-4 comparing the ratio to the predetermined value comprises comparing the ratio to a previously computed ratio determined on a previous iteration by the respective processing block to be nearer to

the optimum value than a predetermined value of the previous iteration (e.g. paragraph [0005]).

Re claim 13, the admitted prior art further discloses in pages 2-4 selecting one of the computed value and the predetermined value that is nearer to the optimum value comprises selecting the greater of the computed value and the predetermined value (e.g. paragraph [0005]).

Re claim 14, the admitted prior art further discloses in pages 2-4 the set of values comprises buffer elements obtained from buffers accessible by the respective processing blocks, and wherein selecting one of the computed value and the predetermined value that is nearer to the optimum value comprises: storing as the predetermined value in a storage medium accessible by the respective processing block one of the computed value and the predetermined value that is nearer to the optimum value (e.g. paragraph [0005], particularly first nine lines and it is performed in hardware); and repeating the elements of computing, comparing, and selecting until all available buffer elements have been accessed (e.g. paragraph [0005], particularly last two lines and it is performed in hardware).

Re claim 15, the admitted prior art further discloses in pages 2-4 determining which of the selected values among the processing blocks is nearest to the optimum value comprises: if there are two selected values, repeating the elements of comparing and selecting in a processing block, with the first selected value as the predetermined value and the second selected value as the computed value (e.g. paragraph [0005], particularly first nine lines); and if there are more than two selected values, repeating in parallel

processing blocks the elements of comparing and selecting, with the first selected value as the predetermined value and the second selected value as the computed value for each respective processing block (e.g. paragraph [0005], particularly last two lines).

Re claim 16, it is a medium claim having similar limitations cited in claim 1. Thus, claim 16 is also rejected under the same rationale as cited in the rejection of rejected claim 1.

Re claim 17, it is a medium claim having similar limitations cited in claim 4. Thus, claim 17 is also rejected under the same rationale as cited in the rejection of rejected claim 4.

Re claim 19, it is a medium claim having similar limitations cited in claim 6. Thus, claim 19 is also rejected under the same rationale as cited in the rejection of rejected claim 6.

Re claim 20, it is a medium claim having similar limitations cited in claim 7. Thus, claim 20 is also rejected under the same rationale as cited in the rejection of rejected claim 7.

Re claim 21, the admitted prior art further discloses in pages 2-4 content to provide instructions to cause the electronic device to select one of the computed value and the predetermined value that is nearer to the optimum value comprises the content to provide instructions to cause the electronic device to (e.g. paragraph [0005]): if a maximum value is searched for, select the computed value if the first product minus the second product is greater than zero, otherwise selecting the predetermined value (e.g. expression 3 in page 3); and if a minimum value is searched for, select the computed

value if the first product minus the second product is less than zero, otherwise selecting the predetermined value (e.g. expression 4 in page 3).

Re claim 22, it is a medium claim having similar limitations cited in claim 11. Thus, claim 22 is also rejected under the same rationale as cited in the rejection of rejected claim 11.

Re claim 23, it is a medium claim having similar limitations cited in claim 12. Thus, claim 23 is also rejected under the same rationale as cited in the rejection of rejected claim 12.

Re claim 24, it has similar limitations cited in claim 1. Thus, claim 24 is also rejected under the same rationale as cited in the rejection of rejected claim 1.

Re claim 25, it has similar limitations cited in claim 2. Thus, claim 25 is also rejected under the same rationale as cited in the rejection of rejected claim 2.

Re claim 26, the admitted prior art further discloses in pages 2-4 separating the elements into the number of different sets comprises separating the elements into a number of different sets (e.g. as product terms in expression 3 or 4 in page 3), the number determined, at least in part, by a number of separate buffer elements fit simultaneously on a data transfer bus from a memory to the processing units (e.g. inherently).

Re claim 27, the admitted prior art further discloses in pages 2-4 for ratio maximization: computing the first product comprises computing the multiplication of an element of the vector A of numerator elements by a denominator member of the initial value pair (e.g. $n_1 * d_{max}$ in expression 3 in page 3); and computing the second product comprises computing the multiplication of an element of the vector B of denominator

elements by a numerator member of the initial value pair (e.g. $n_{max}*d_1$ in expression 3 in page 3).

Re claim 28, the admitted prior art further discloses in pages 2-4 vector A comprises a correlation vector and vector B comprises an energy vector (e.g. paragraphs [0002-0005] as actual received signal).

Re claim 29, the admitted prior art further discloses in pages 2-4 for ratio minimization: computing the first product comprises computing the multiplication of an element of the vector A of denominator elements by a numerator member of the initial value pair(e.g. n_1*d_{min} in expression 4 in page 3); and computing the second product comprises computing the multiplication of an element of the vector B of numerator elements by a denominator member of the initial value pair (e.g. $n_{min}*d_1$ in expression 4 in page 3).

Re claim 30, it has similar limitations cited in claim 15. Thus, claim 30 is also rejected under the same rationale as cited in the rejection of rejected claim 15.

Re claim 31, it is an apparatus having similar limitations cited in claim 24. Thus, claim 31 is also rejected under the same rationale as cited in the rejection of rejected claim 24.

Re claim 32, the admitted prior art discloses in pages 2-4 a memory to store vectors A and B (e.g. in page 3-4), but fails to disclose communicatively coupled with parallel processing units via a direct memory access (DMA) channel. However, the examiner takes an official notice that the DMA channel is well-known in the art at the technology and widely used in many practical applications.

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add the DMA channel into the admitted prior art's invention because it would enable to increase the transferring throughput.

Re claim 33, it has similar limitations cited in claim 25. Thus, claim 33 is also rejected under the same rationale as cited in the rejection of rejected claim 25.

Re claim 34, it has similar limitations cited in claim 26. Thus, claim 34 is also rejected under the same rationale as cited in the rejection of rejected claim 26.

Re claim 35, the admitted prior art discloses in pages 2-4 the data transfer bus comprises a 64-bit bus, and the elements of vectors A and B comprise 16-bit values (e.g. standard or typical).

Re claim 36, it has similar limitations cited in claim 27. Thus, claim 36 is also rejected under the same rationale as cited in the rejection of rejected claim 27.

Re claim 37, it has similar limitations cited in claim 29. Thus, claim 37 is also rejected under the same rationale as cited in the rejection of rejected claim 29.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. U.S. Patent No. 2005/0065785 to Bessette discloses an indexing pulse positions and signs in algebraic codebooks for coding of wideband signals.

b. U.S. Patent No. 6,748,405 to de Tremiolles et la. disclose a method and circuits for performing the quick search of the minimum/maximum value among a set of numbers.

c. U.S. Patent No. 5,598,354 to Fang et al. disclose a motion vidoe compression system with neural network having winner-take-all function.

d. U.S. Patent No. 6,115,725 to Shibata et al. disclose a semiconductor arithmetic appratus.

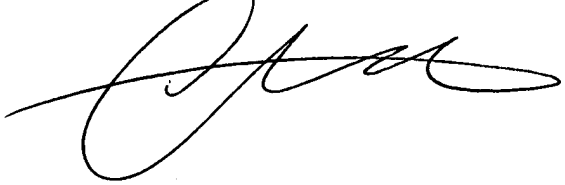
e. U.S. Patent No. 5,968,198 to Hassan et al. disclose a decoder utilizing soft information output to minimize error rates.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (571) 272-3721. The examiner can normally be reached on M => F from 7:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chat C. Do



Examiner
Art Unit 2193

December 17, 2007